LEE -- 10/733,276
Client/Matter: 040044-0307078

REMARKS

Claims 2, 8, 9, 11, 13 and 14 are pending. By this Amendment, claims 4 and 5 are canceled without prejudice or disclaimer and claims 2, 8 and 13 are amended. Reconsideration and allowance in view of the above amendments and the following remarks are respectfully requested.

Entry of the Amendment is proper under 37 C.F.R. § 1.116 because the amendments: (a) place the application in condition for allowance for the reasons discussed herein; (b) do not present any new issues that would require further consideration and/or search as they merely amplify issues discussed throughout prosecution (for example, the subject matter of the amendment to claim 8 was previously considered in relation to claim 4 as originally filed, and the amendments to claim 13 were previously considered in relation to claim 8 as originally presented); (c) do not add any additional claims without canceling a corresponding number of claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented as they are in response to arguments raised in the final rejection. Entry of the Amendment is respectfully requested.

Claims 4, 8 and 13 were rejected under 35 U.S.C. § 102(b) over Lin (U.S. Patent No. 6,218,303). The rejection is respectfully traversed.

Claim 8 recites a method of manufacturing a semiconductor device comprising forming a first insulating layer on a semiconductor substrate; forming a first conductive line by depositing a conductive material on the first insulating layer and selectively patterning the conductive material; forming a second insulating layer by depositing an insulating material on top of the substrate including on the first conductive line; forming a via hole and a trench by selectively patterning the second insulating layer to expose a certain portion of the first conductive line; removing a natural oxide layer, formed on the first conductive line through natural oxidation of the first conductive line, by heat treating in an H_2+CO gas atmosphere; forming a metal barrier by depositing a metal layer on top of the substrate including in the via hole and on the trench; forming a copper seed layer on top of the metal barrier; and removing a natural copper oxide layer, formed on the copper seed layer through natural oxidation of the copper oxide layer, by heat treating in an H_2+CO gas atmosphere.

Lin does not disclose or suggest the method recited in claim 8. Lin does not disclose the claimed formation of the first conductive line. As set forth in claim 8, the first conductive line is

formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material.

In response to Applicant's arguments that Lin does not disclose or suggest this feature, the Examiner on page 5, second paragraph, of the March 30, 2005 Office Action, states that Lin "clearly teaches selectively pattern a conductive material deposited on the first insulating layer (layer 56 is selectively pattern because its pattern forms only in the opening not any other place (see figure 3 for detail wherein the metal forms only in the opening))."

Lin discloses, in column 3, lines 40-46, that the intermetal dielectric layer 42, an insulating layer, is photolithographically patterned at step S13 to define trenches 74 that will contain second metal conductors 60 and via apertures 76 that will contain intermetal layer vias 62, as shown in Fig. 3. The bulk of the material removed in intermetal dielectric patterning step S13 is silicon dioxide, however, silicon nitride at the base of the via apertures is removed to expose an area of first copper sublayer 56.

As the above passage of Lin makes clear, it is the intermetal dielectric layer 42 that is patterned, not the copper sublayer 56. The copper sublayer is only exposed after the intermetal dielectric layer 42 is patterned and the portions of the intermetal dielectric layer 42 that are photolithographically patterned are removed. Exposing portions of the copper sublayer 56 are not the same as patterning the copper sublayer 56.

In the art of semiconductor manufacture, the terms "pattern" and "patterning", when used as verbs, have a meaning to those of ordinary skill in the art that connotes the process used in photolithography, namely the covering of the material with a photoresist, exposure to a certain wavelength of light projected in a certain pattern so that the portions of the photoresist exposed to the patterned radiation become soluble, and the removal of the soluble portions of the photoresist followed by processing, including for example etching, of the material. According to this understanding of the terms "pattern" and "patterning", one of ordinary skill in the art would understand that the intermetal dielectric layer 42 (an insulating layer) of Lin is patterned. One of ordinary skill in the art would not interpret the exposure of the copper sublayer 56 caused by the patterning of the intermetal dielectric layer 42 as "patterning" of the copper sublayer 56. Such an interpretation as relied upon by the Examiner is not consistent with the interpretation of the term "patterning" that one of ordinary skill in the art would reach. See MPEP § 2111.

Claim 8 also recites removing a natural oxide layer, formed on the first conductive line through natural oxidation of the first conductive line, by heat treating in an H_2+CO gas atmosphere and removing a natural oxide layer, formed on the copper seed layer through natural oxidation of the copper seed layer, by heat treating in an H_2+CO gas atmosphere. Lin does not disclose or suggest these two natural oxide layer removals.

Claims 2 and 9 recite additional features of the invention and are allowable for the same reasons as discussed above with respect to claim 8 and for the additional features recited therein.

Claim 13 recites a method of manufacturing a semiconductor device comprising forming a first insulating layer on a semiconductor substrate; forming a first conductive line by depositing a conductive material on the first insulating layer and selectively patterning the conductive material; forming a second insulating layer by depositing an insulating material on top of the substrate including on the first conductive line; forming a via hole and a trench by selectively patterning the second insulating layer to expose a certain portion of the first conductive line; removing a natural oxide layer, formed on the first conductive line through natural oxidation of the first conductive line, by heat treating in an H_2+CO gas atmosphere; forming a metal barrier by depositing a metal layer on top of the substrate including in the via hole and on the trench; forming a copper seed layer on top of the metal barrier; removing a natural copper oxide layer, formed on the copper seed layer through natural oxidation of the copper seed layer, by heat treating in an H2+CO gas atmosphere; depositing a conductive material for forming a conductive line on top of the substrate including on the metal barrier and the copper seed layer to sufficiently fill the via hole and the trench; forming a plug and a second conductive line by planarizing the conductive material on the second insulating layer in order to expose the second insulating layer; and removing a natural oxide layer, formed on the second conductive line through natural oxidation of the second conductive line, by heat treating in an H_2+CO gas atmosphere.

Lin does not disclose or suggest the method recited in claim 13. As discussed above, Lin does not disclose the claimed formation of the first conductive line by patterning the conductive material. Lin patterns the intermetal dielectric layer 42, which is an insulating layer, not a conductive layer.

Claim 13 also recites removing a natural oxide layer, formed on the first conductive line through natural oxidation of the first conductive line, by heat treating in an H_2+CO gas

atmosphere; removing a natural oxide layer, formed on the copper seed layer through natural oxidation of the copper seed layer, by heat treating in an H_2+CO gas atmosphere; and removing a natural oxide layer, formed on the second conductive line through natural oxidation of the second conductive line, by heat treating in an H_2+CO gas atmosphere. Lin does not disclose or suggest these three natural oxide layer removals.

Claims 11 and 14 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 13 and for the additional features recited therein.

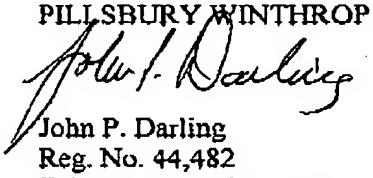
Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) over Lin are respectfully requested.

In view of the above amendments and remarks, Applicant respectfully submits that all of the claims are allowable and that the entire application is in condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
PILLSBURY WINTHROP SHAW PITTMAN LLP



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